Low cost, high performance and reliable 90nm CMOS process for automotive products with NVM and HV options

Low Cost

- 90nm CMOS process + 3.3V
- 1-3 additional masks for 1.5μ^2single poly NVM cell
- 0-2 additional masks for LDmos
- No SOI nor EPI just standard CMOS substrate
- Cheap process install due to device optimization only

High quality

- No SOI: standard CMOS performance on ESD, Latch-up, GOI
- No new oxide: no new gate ox integrity issues
- No new transistor family for NVM therefore no new issues and forbidden biases

High Performance

90nm CMOS 100% compatible process (3.3V process option required)

LDmos

- Fully isolated (patented process)
- BV up to 120V compatible with state of the art LDmos on SOI
- High current due to deep trenches (2 - 10 micron)
- Re-use of existing libraries in some cases possible

Non-volatile memory

- Superior to standard NVM due to advanced tunnel mechanism (patented)
- Fast and low-power due to advanced architecture (patented)
- High data retention and cycling performance due to different F/N tunneling path for program and erase

State of the art

- Patents filed
- Development plan of 1 year including first product (if design is ready)
- CMOS PDK available from FAB
- Device dimensions to optimize depending on customer specs.

SemiConsultor

- 1 person company
- 20+ years in micro-electronics device & process development
- 6 owned patents (2 NVM, 1 HV, 3 imaging)
- Specialized in low cost device options in CMOS

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