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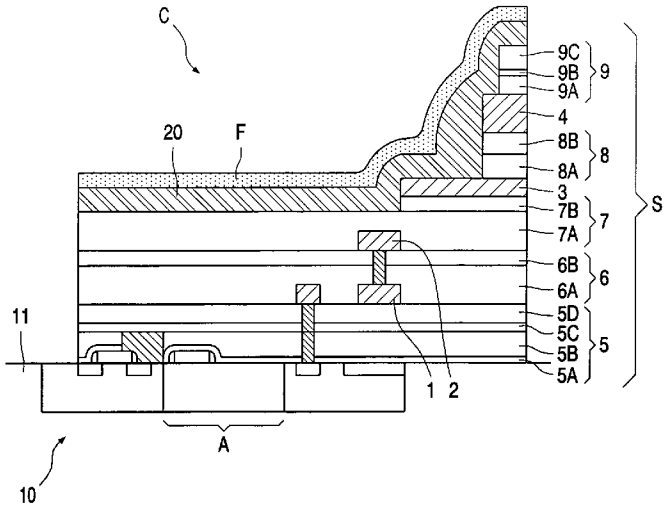
(54) Title: OPTO-ELECTRONIC SEMICONDUCTOR DEVICE, METHOD OF MANUFACTURING SAME, AND CAMERA PROVIDED WITH SUCH A DEVICE



(57) Abstract: The invention relates to a method of manufacturing an opto-electronic semiconductor device (10) with a substrate and a semiconductor body (1) whereby a CMOS image sensor is formed with a matrix of radiation-sensitive areas (A) that form pixels of the sensor and whereby on the semiconductor body (11) a stack (S) is formed of alternatingly an electrically insulating layer (5,6,7,8,9) and a patterned conducting layer (1,2,3,4). According to the invention, after the formation of the stack (S) of electrically insulating and patterned conducting layers (1-9), cavities (C) are formed in the stack (S) above the radiation-sensitive areas (A) by removing at these locations a part of the stack (S) with the aid of, preferably wet, etching, such that the surface of the stack (S) outside the cavities (C) is protected with a mask (M1). In this way image sensors (10) are obtained with a high sensitivity and with a low (color) crosstalk.

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Opto-electronic semiconductor device, method of manufacturing same, and camera provided with such a device

The invention relates to an opto-electronic semiconductor device with a substrate and a semiconductor body, often made of silicon, in which a (C)MOS image sensor is formed with a matrix of radiation-sensitive regions which form pixels of the image sensor, and in which a stack of layers is formed on the semiconductor body, comprising in alternation an electrically insulating layer and a patterned electrically conducting layer. A (C)MOS (= Complementary Metal Oxide Semiconductor) image sensor is understood to be a solid-state image recording device which is manufactured by means of (standard) CMOS technology. Such a technology is advantageously used in the manufacture of ICs (= Integrated Circuits) comprising MOSFETs (= Field Effect Transistors), often in large numbers. A CMOS image sensor often comprises, besides a small number of such transistors for each pixel, also an integrated circuit with transistors and other components, for example for signal processing and management, outside the matrix of pixels. The radiation-sensitive region may form, for example, a transistor or diode, or be part thereof.

US 6,506,619 describes a method of manufacturing a CMOS image sensor wherein a matrix of radiation-sensitive regions in the form of photodiodes is formed in a semiconductor body of silicon which at the same time acts as a substrate. One or several MOSFETs are coupled thereto, for example acting as transfer or reset transistors. The image sensor is manufactured in a multilayer process. A stack of layers is provided on the semiconductor body in this case, comprising in alternation an electrically insulating or dielectric layer, and a patterned electrically conducting layer, often made of a metal or metal alloy or metal compound. Patterning of the conductive layer may be linked to the circumstance that it often does not transmit the radiation to be detected and should accordingly be provided with openings at the areas of the radiation-sensitive regions, or to the function of the electrically conducting layers, which often constitute a multilayer wiring for the device.

It is a disadvantage of the known method and semiconductor device that a trend towards ever smaller dimensions of the smallest details (progressing from

approximately 1 μm down to approximately 0.1 μm) and the use of a larger number of insulating and conducting layers do not lead to CMOS image sensors with good properties in all respects in practice. Thus the sensitivity is not always as high as desired, and in addition crosstalk, in particular of different colors, may occur between two neighboring pixels where filters for different colors are present above the radiation-sensitive regions of neighboring pixels.

It is accordingly an object of the present invention to provide CMOS image sensors with a high sensitivity and a low (color) crosstalk. The method of manufacturing them is then preferably compatible with standard CMOS technology, also in the case of smallest dimensions that become continually smaller.

The invention is defined by the independent claims. The dependent claims define advantageous embodiments. According to the invention, a method of the kind mentioned in the introductory text is characterized in that, after the stack of electrically insulating and conducting layers has been provided, a cavity is formed in the stack at the areas of the radiation-sensitive regions in that a portion of the stack is removed again, while the portion of the stack situated outside the cavity to be formed is protected by a mask. The removal of a portion of the stack may take place, for example, by means of etching, but also by alternative known means, for example in that a laser beam is directed at the stack, so that the latter evaporates.

The invention is based on the recognition first of all that the lower sensitivity and in particular color crosstalk are the result of the comparatively great thickness of the stack of layers on which the color filter layers are present. A slight angular deviation of the incident radiation, such as light, may have the result that radiation destined for a certain pixel arrives at a neighboring pixel which is provided, for example, with a color filter for a different color. In addition, said comparatively great thickness of the stack implies that higher absorption losses occur therein and also more losses owing to reflections against boundary surfaces, because a thicker stack means in practice that there are a larger number of boundary surfaces between the individual layers. The invention is furthermore based on the recognition that these disadvantages can be counteracted through the removal of part of the stack at the area of the radiation-sensitive region at the end of the manufacturing process while using a mask for the rest of the surface of the stack. This has various advantages over, for example, trying to make the stack thinner or making separate openings in individual layers of the stack,

such as a high yield, smaller process deviations, and the possibility of using properties, whether or not purposely introduced, of the stack in the formation of the cavity.

In a first embodiment of a method according to the invention, the pattern in the electrically conducting layers is chosen such that the walls of the cavity are given a stepped profile in the formation of the cavity.

Such a profile offers potential advantages in the provision of the color filter layers in the bottom of the cavity, because it makes it easier to cover this bottom with a layer that is as homogeneous as possible. This is because such a layer will tend to be thicker or thinner adjacent the corner point between bottom and wall than close to the center of the bottom if the walls of the cavity are steeper. In principle, a smooth, non-steep gradient of the cavity wall would also be suitable for this purpose. The method of this embodiment, however, is better suited to a process with increasingly smaller dimensions and more compatible with existing processes. If etching techniques are chosen for forming the cavity, a wet-chemical etching process is preferred to a so-called plasma or dry etching process.

An etchant is preferably chosen for etching with which the materials of the electrically insulating layers are selectively etched with respect to the materials of the conducting layers. Since the etching stops upon reaching a metal layer or portion thereof, the desired stepped profile of the cavity as discussed above may be readily formed in particular through the use of the pattern in such conducting layers.

In a favorable embodiment, one of the electrically conducting layers is provided above the radiation-sensitive region in an uninterrupted manner, and a further mask is provided on this layer, covering a portion thereof, after said layer has been reached by the etching process, whereupon the exposed portion of said layer is removed by means of a suitable etchant, after which etching is continued. A step desired for the stepped profile is formed in a simple manner thereby.

In a further embodiment, in which one of the electrically conducting layers is provided above the radiation-sensitive region in an uninterrupted manner, etching is performed by means of the mask down to said conducting layer, whereupon the exposed portion thereof is removed with the use of the same mask and a suitable etchant, after which etching is continued. In this modified embodiment, the profile of the cavity is indeed steeper, but this embodiment has the advantage that the desired cavity can be formed with no more than one mask.

In another modified embodiment, the stack may be provided with a layer, which may or may not perform a function in the CMOS process, but which acts as an etch

stop layer in the formation of the cavity. A step in the wall of the cavity may again be formed in a similar manner in this case.

Preferably, a color filter layer is provided in the cavity after the formation thereof. A color imaging unit is thus formed with excellent properties such as a high sensitivity and a low (color) crosstalk.

Preferably, furthermore, lenses acting as diaphragms are provided above the radiation-sensitive regions.

In a favorable embodiment, a stack is used which comprises four or more conducting layers and which accordingly comprises four or more dielectric layers. The two lowermost conducting layers then serve, for example, for forming a multilayer pattern of (connection) conductors, possibly with the use of so-termed vias in one or more dielectric layers for interconnecting the conductors or for connecting them to semiconductor regions that form part of the device. The two uppermost conducting layers, which preferably comprise aluminum or copper or an alloy thereof, may then serve as connection regions, for example for wire connectors. One or both of these layers may also be used for screening a portion of the device against incident radiation. In particular, this may relate to a portion that is provided with integrated electronic (accessory) circuits.

In such a modified embodiment, the depth for the cavity is chosen such that the desired result is achieved. This may already be the case, for example, with a reduction of the thickness of the stack, for example approximately 6 μm thick, down to a thickness of approximately 3 μm. The cavity may thus be advantageously formed down to an electrically insulating layer which is present on the second conducting layer. In another favorable modification, the cavity is formed down to an electrically insulating layer which is present below the second conducting layer.

The invention further relates to an opto-electronic semiconductor device comprising a substrate and a semiconductor body which is provided with a solid-state image sensor comprising a matrix of radiation-sensitive regions which form pixels of the image sensor, with a stack of layers provided on the semiconductor body, which stack comprises an alternation of an electrically insulating layer and a patterned electrically conducting layer each time, characterized in that the stack of electrically insulating and conducting layers has cavities at the areas of the radiation-sensitive regions. This has the advantage that there is less color crosstalk and that the absorption losses in the stack are lower.

Such a device can be inexpensive and compact and is furthermore particularly suitable for applications in which a low power consumption of the device is desired.

The invention further relates to a camera provided with an opto-electronic semiconductor device according to the invention. Such a camera may be used to advantage in, for example, a laptop computer or a mobile telephone. The use in high-quality photocameras is also possible.

The invention will now be explained in more detail with reference to a few embodiments and the drawing, in which:

Figs. 1 to 6 show an opto-electronic semiconductor device diagrammatically and in a cross-section perpendicular to the thickness direction in consecutive relevant stages of its manufacture by means of a first embodiment of a method according to the invention,

Figs. 7 to 10 show an opto-electronic semiconductor device diagrammatically and in a cross-section perpendicular to the thickness direction in consecutive relevant stages of its manufacture by means of a second embodiment of a method according to the invention, and

Figs. 11 to 12 show an opto-electronic semiconductor device diagrammatically and in a cross-section perpendicular to the thickness direction in consecutive relevant stages of its manufacture by means of a third embodiment of a method according to the invention.

The Figures are not drawn true to scale and some dimensions, such as dimensions in the thickness direction, have been particularly exaggerated for greater clarity. Corresponding regions or components have been given the same hatchings or the same reference symbols as much as possible in the various Figures.

Figs. 1 to 6 show an opto-electronic semiconductor device diagrammatically and in a cross-section perpendicular to the thickness direction in consecutive relevant stages of its manufacture by means of a first embodiment of a method according to the invention, The formation of the device 10 (see Fig. 1) starts with a semiconductor body 11 with a substrate which is not separately indicated in the drawing, which is made of silicon here, and in which a radiation-sensitive region A is formed. The radiation-sensitive region A is, for example, an n-type silicon region which together with a p-type silicon region, for example situated below it and not shown in the drawing, forms a radiation-sensitive photodiode. Four transistors are present for each pixel in the device of this example, of which two T1, T2 are (partly) visible in the cross-section of Fig. 1 and which serve for transferring and amplifying

the signals and for resetting and selecting the pixels. The device 10 in this example comprises four conducting layers 1, 2, 3, 4 below which, between which, and above which dielectric layers 5, 6, 7, 8, 9 are present in this case, which comprise, for example, a silicon dioxide (layers 5B, 5C, 5D, 6B, 7B, 8A, 8B, 9A, 9B, 9C), a silicon nitride (layer 5A), or a so-termed "low-k" material (layers 6A, 7A).

The first two conducting layers 1, 2 are connected to one another or to semiconductor regions in the semiconductor body 11 by means of vias V. The two uppermost conducting layers 3, 4, made of aluminum here, may form a screen against radiation incident on the device 10 on the right of the line L. In this example, the third conducting layer 3 is initially present uninterrupted, as is visible in Fig. 1, both in the region on the right of the line L and on the left thereof, where the radiation-sensitive region A is present. The device 10 in this example is manufactured by a standard CMOS technology up to the stage of manufacture shown in Fig. 1. The portion of the device 10 shown in Fig. 1 represents the transition between two portions of the device. A first portion, on the left of the line L1 in Fig. 1, where the matrix of radiation-sensitive regions A is present, and a second portion, on the right of the line L1 in Fig. 1, where one or more electronic circuits are present which are to be protected against incident radiation. This second portion surrounds the first portion here. The drawing only shows the transition zone. The lateral dimensions of the matrix of radiation-sensitive regions A are, for example, approximately 5 mm x 5 mm, while the total device 10 measures approximately 10 mm x 10 mm. Said second portion then forms an approximately 2.5 mm wide strip of the semiconductor body surrounding the matrix of radiation-sensitive regions A. The stage shown in Fig. 1 in this standard CMOS manufacture is the stage just before the application of the scratch protection in the form of a silicon nitride layer.

According to the invention (see Fig. 1), a mask M1, made of photoresist in this case, is first applied by means of photolithography and etching. Then the device 10 is introduced into a plasma etching apparatus and the insulating layers 9A, 9B, 9C are removed in a dry, anisotropic etching process within the opening of the mask M1. The fourth metal layer 4 (see Fig. 2) acts as an etch stop layer here, but etching continues within the opening in the metal layer 4. The dielectric layers 8A, 8B are thus locally removed. A cavity C is formed thereby at the area of the active region A in the stack S of conducting and dielectric layers 1 to 9. The etching process stops again upon reaching the third metal layer 3.

Subsequently (see Fig. 3), a second mask M2 is provided on the device 10, exposing a smaller portion of the third metal layer 3 than corresponds to the opening in the second metal layer 4. The exposed portion of the third metal layer 3 is subsequently removed

by etching with a different etchant, whether or not selectively with respect to a subjacent dielectric layer 7B. Etching is then continued (see Fig. 4) with an etchant suitable for etching the dielectric layers 7A, 7B, such that a cavity C arises in the stack S having a depth of slightly more than half the entire stack S, which is approximately 6 μm thick here.

The masks M1 and M2 (see Fig. 5) are subsequently removed in a usual manner. A scratch protection in the form of a silicon nitride layer 20 is first provided. Then (see Fig. 6) a color filter layer F is provided in the bottom of each cavity C in a spin process or in a spray process. Three different filters are used in neighboring pixels in the case of a color image sensor. This is done in that three filter layers are provided which are patterned by means of photolithography. Subsequently, lenses (not shown) are provided above each radiation-sensitive region A of the image sensor 10.

The method according to the invention provides an image sensor 10 with a comparatively high sensitivity on the one hand and with no or only a very slight (color) crosstalk between neighboring pixels on the other hand owing to the smaller thickness of the stack S below the filter F. Since the profile of the walls of the cavity C, of which only one is shown in the drawing for simplicity's sake, has a stepped shape, the filter layer F on the bottom of the cavity C can have a comparatively uniform thickness, whereby the quality of the image sensor 10 is improved. The device 10 of this example is ready for final mounting after the lenses mentioned above have been applied.

Figs. 7 to 10 show an opto-electronic semiconductor device diagrammatically and in a cross-section perpendicular to the thickness direction in consecutive relevant stages of its manufacture by means of a second embodiment of a method according to the invention, The manufacture of the device 10 in this example largely proceeds as in the preceding example up to the stage shown in Fig. 7. The main difference is that the third metal layer 3 is patterned by means of photolithography and etching immediately after its provision during the realization of the stack S. This is generally possible without an additional mask being necessary. This is because the third metal layer 3 will have to be patterned already in a portion of the device 10 situated outside the drawing, and the mask required for this can be adapted. Any imperfection in the conformity of the dielectric layers 8, 9 provided above the third metal layer could, however, normally lead to problems.

In a method according to the invention, in this embodiment, such imperfections play no part because in a later stage the cavity C will be made in this location, so that said imperfections are removed.

After the stack S (see Fig. 7) has been completed, the manufacture largely proceeds as in the preceding example. The main difference is that the etching process need not be interrupted or modified in the stage in which the third metal layer 3 (see Fig. 8) is reached. In this example (see Fig. 9), the formation of the cavity is continued until the second, patterned metal layer 2 is reached. A dielectric layer 6B situated below the second metal layer 2 may possibly be used as an etch stop layer during this. If so desired, a very thin layer of silicon nitride (not shown) may be provided on the silicon dioxide layer 6B for this purpose during the formation of the stack S in addition to said layer 6B of silicon dioxide shown in the example. The manufacture of this modified embodiment (see Fig. 9) also utilizes a pattern present in the second conducting layer 2 during the formation of the stepped profile in the wall(s) of the cavity C. This means that the cavity C comprises a greater number of raised steps H situated on the bottom of the cavity C between neighboring pixels in addition to a second wall which lies to the left of the drawing and which is identical to the wall visible in the right of the drawing. Finally (see Fig. 10), manufacture is continued as discussed above for the first example, and color filters F are provided in the cavities C.

Figs. 11 and 12 show an opto-electronic semiconductor device diagrammatically and in a cross-section perpendicular to the thickness direction in consecutive relevant stages of its manufacture by means of a third embodiment of a method according to the invention, The only difference with the preceding example is the fact that the strips of the metal layer 3 used therein (see Figs. 7 and 10 which correspond to the stages of Figs. 11 and 12), which are present on the left in the drawing, are absent. The profile H forming a local elevation of the bottom of the cavity C is accordingly less high and profiled (for example, see Fig. 12) than that of the device of Fig. 10. An advantage of this modification is that the lacquer of the color filter layer can have a better adhesion.

It is possible again in this modification of a method according to the invention, which subsequently proceeds in the same manner as that of the second example, to use a (dielectric) etch stop layer, if so desired.

The invention is not limited to the described embodiments, since many variations and modifications are possible to those skilled in the art within the scope of the invention. Thus the devices may be manufactured with different geometries and/or different dimensions. Instead of a Si substrate, a substrate of glass, ceramic material, or synthetic resin may be used. The semiconductor body may be formed by means of the so-termed SOI (= Silicon On Insulator) technology. A so-termed substrate transfer technique may or may not be used for this.

It is further noted that materials other than those mentioned in the examples may be used within the scope of the invention. This holds both for the conducting (or metal) layers and/or the dielectric layers. It is also possible to use different materials for layers of the same type. Also, different deposition techniques may be used for said layers or materials: epitaxy, CVD (= Chemical Vapor Deposition), sputtering, and vaporizing. Instead of wet-chemical etching methods, for example HF-based solutions for layers comprising silicon oxide and (hot) phosphoric acid for silicon nitride, use may be made of a dry etching method for the removal of one or several of the layers forming part of the stack.

It is once more noted, furthermore, that the device may comprise further active and passive semiconductor elements or electronic components, such as a larger number of diodes and/or transistors, and resistors and/or capacitors, whether or not in the form of an integrated circuit.

The invention is not limited to CMOS image sensors. Other technologies, such as CCD, are also covered thereby.

CLAIMS:

1. An opto-electronic semiconductor device (10), comprising a substrate and a semiconductor body (11) which is provided with a solid-state image sensor comprising a matrix of radiation-sensitive regions (A) which form pixels of the image sensor, with a stack (S) of layers provided on the semiconductor body, which stack comprises an alternation of an electrically insulating layer (5, 6, 7, 8, 9) and a patterned electrically conducting layer (1, 2, 3, 4) each time, characterized in that the stack (S) of electrically insulating and conducting layers has cavities (C) at the areas of the radiation-sensitive regions (A).

2. A semiconductor device (10) as claimed in claim 1, characterized in that the walls of the cavity (C) are provided with a stepped profile.

3. A semiconductor device (10) as claimed in any one of the preceding claims, characterized in that it is provided with a color filter layer (F) in the cavity (C).

4. A semiconductor device (10) as claimed in any one of the preceding claims, characterized in that it is provided with lenses above the radiation-sensitive regions (A).

5. A semiconductor device (10) as claimed in any one of the preceding claims, characterized in that the stack (S) comprises four or more conducting layers (1, 2, 3, 4).

6. A semiconductor device (10) as claimed in any one of the preceding claims, characterized in that the cavity (C) extends down to the electrically insulating layer (7A) which lies on the second conducting layer (2) in the stack (S), as viewed from the semiconductor body (11).

7. A semiconductor device (10) as claimed in any one of the preceding claims, characterized in that the cavity (C) extends down to the electrically insulating layer (6B) which lies below the second conducting layer (2) in the stack (S), viewed from the semiconductor body (11).

8. A method of manufacturing an opto-electronic semiconductor device (10) with a substrate and a semiconductor body (11), wherein a solid-state image sensor is formed with a matrix of radiation-sensitive regions (A) which form pixels of the image sensor, and wherein a stack (S) of layers is formed on the semiconductor body (11), comprising electrically insulating layers (5, 6, 7, 8, 9) and patterned electrically conducting layers (1, 2, 3, 4) in alternation, characterized in that, after the provision of the stack (S) of electrically insulating and conducting layers, a cavity (C) is formed in the stack at the area of each radiation-sensitive region (A) in that a portion of said stack (S) is removed again in said area.

9. A method as claimed in claim 8, characterized in that the portion of the stack (S) situated outside the cavity (C) to be formed is protected by a mask (M1).

10. A method as claimed in one of the claims 8 and 9, characterized in that the pattern in the electrically conducting layers (3, 4) is chosen such that the walls of the cavity (C) are given a stepped profile during the removal of a portion of the stack (S).

11. A method as claimed in any one of the claims 8 to 10, characterized in that one of the electrically conducting layers (3) is provided uninterrupted above the radiation-sensitive region, and said layer (3) is reached after the removal of a portion of the layers present thereon, and a further mask (M2) is provided thereon so as to cover a portion thereof, whereupon the exposed portion thereof is removed by a suitable technique, after which the formation of the cavity (C) is continued.

12. A method as claimed in any one of the claims 8 to 11, characterized in that one of the electrically conducting layers (3) is provided uninterrupted above the radiation-sensitive region and is removed by means of the mask (M1) down to said conducting layer (3), whereupon the exposed portion thereof is removed in a suitable manner but with the use of the same mask (M1), after which the formation of the cavity (C) is continued.

13. A method as claimed in any one of the claims 8 to 12, characterized in that the removal of the stack (S) takes place by means of etching.

14. A method as claimed in claim 13, characterized in that the cavity (C) is formed by wet-chemical etching methods.

15. A method as claimed in one of the claims 13 and 14, characterized in that an etchant is chosen for the etching by means of which the materials of the electrically insulating layers are selectively etched with respect to the materials of the conducting layers.

16. A method as claimed in any one of the claims 13 to 15, characterized in that the stack (S) is provided with a layer which acts as an etch stop layer in the formation of the cavity (C).

17. A method as claimed in any one of the claims 8 to 16, characterized in that a color filter layer F is provided in the cavity (C) after the formation of the latter.

18. A method as claimed in any one of the claims 8 to 17, characterized in that lenses are provided above the radiation-sensitive regions (A).

19. A method as claimed in any one of the claims 8 to 18, characterized in that the stack (S) is provided with four or more conductive layers (1, 2, 3, 4).

20. A method as claimed in claim 19, characterized in that the cavity (C) is formed down to an electrically insulating layer (7A) which lies on the second conducting layer (2) in the stack (S), viewed from the semiconductor body (11).

21. A method as claimed in claim 19, characterized in that the cavity (C) is formed down to an electrically insulating layer (6B) which is below the second conducting layer (2) in the stack (S), viewed from the semiconductor body (11).

22. A camera comprising an opto-electronic semiconductor device (10) as claimed in any one of the claims 1 to 7.

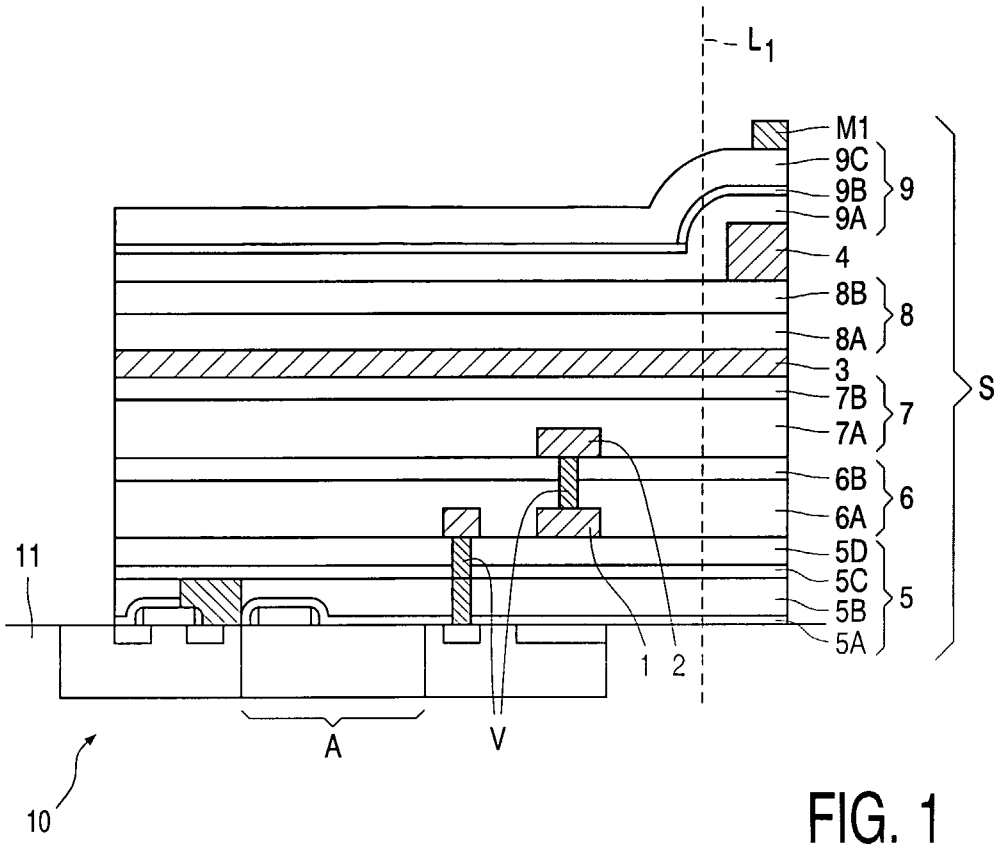
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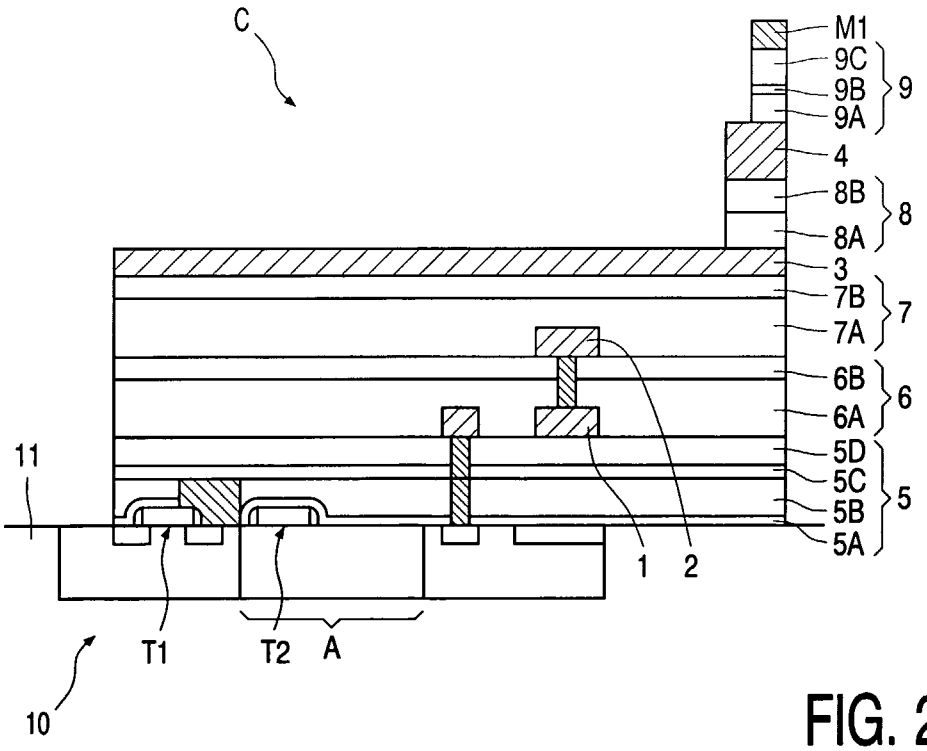
FIG. 1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11
1
2
T1
T2
A
10

FIG. 2

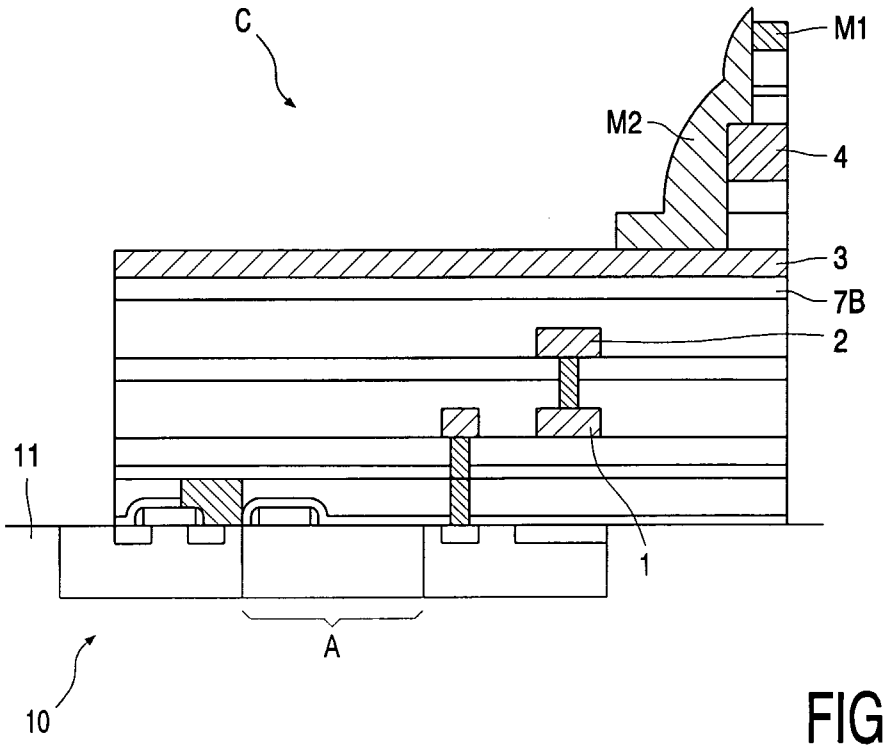


FIG. 3

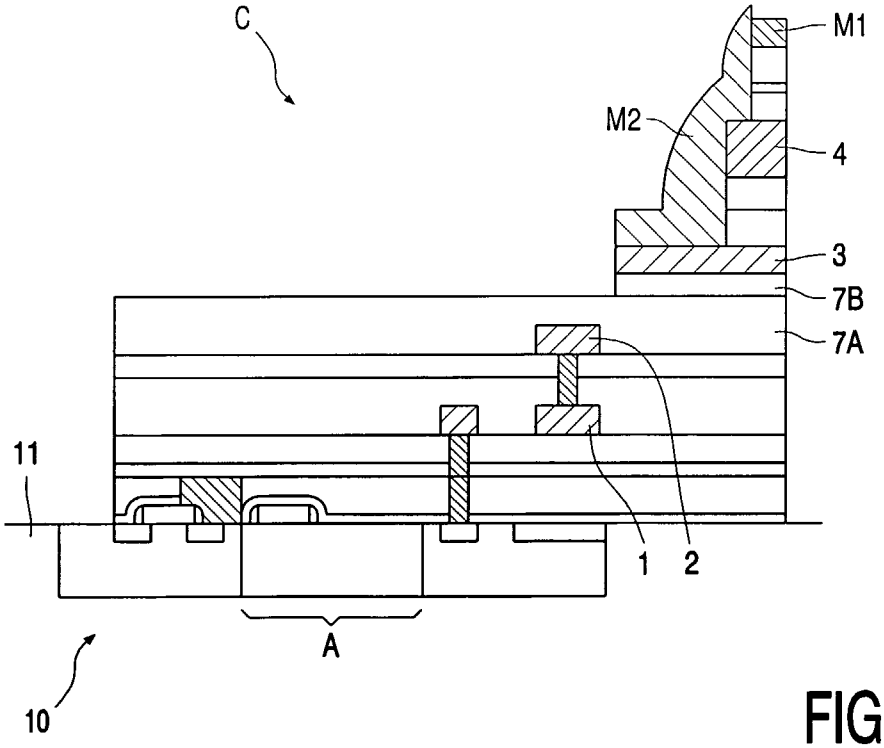
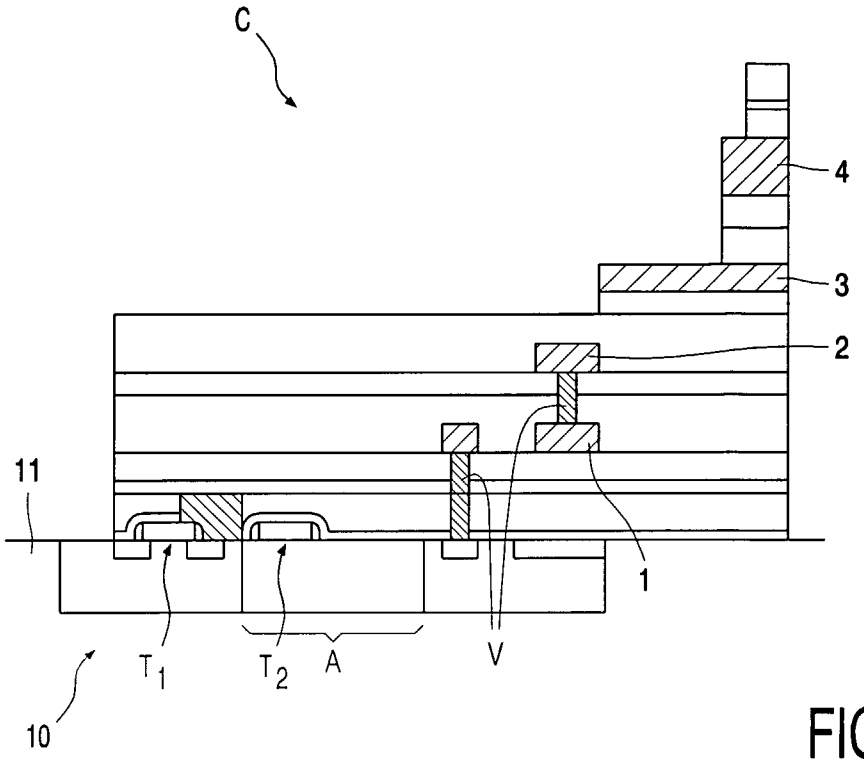


FIG. 4


C
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3
2
11
1
T_1
T_2
A
V
10

FIG. 5

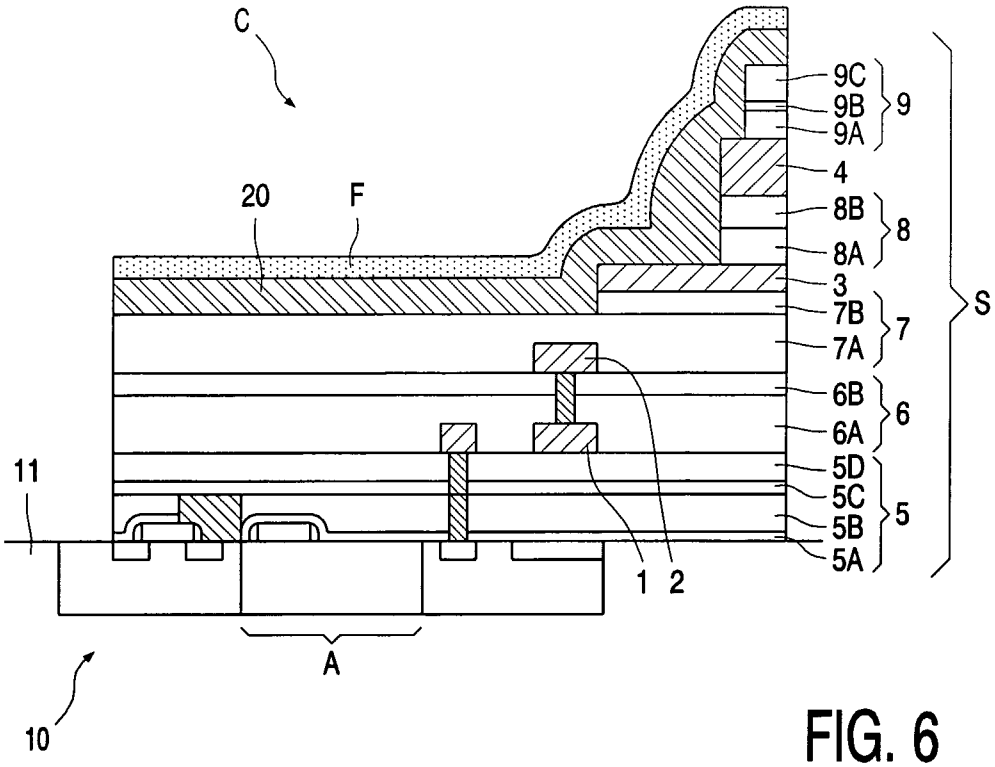

C
9C
9B
9A
9
4
20
F
8B
8A
8
3
7B
7A
7
S
6B
6A
6
11
5D
5C
5B
5A
5
1
2
A
10

FIG. 6

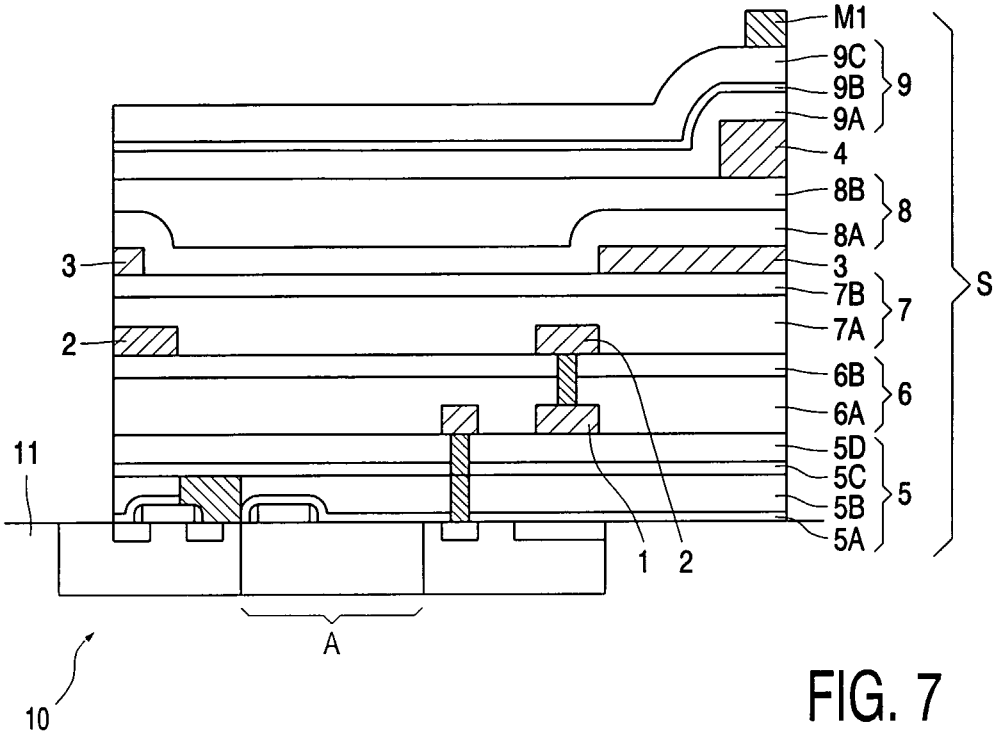
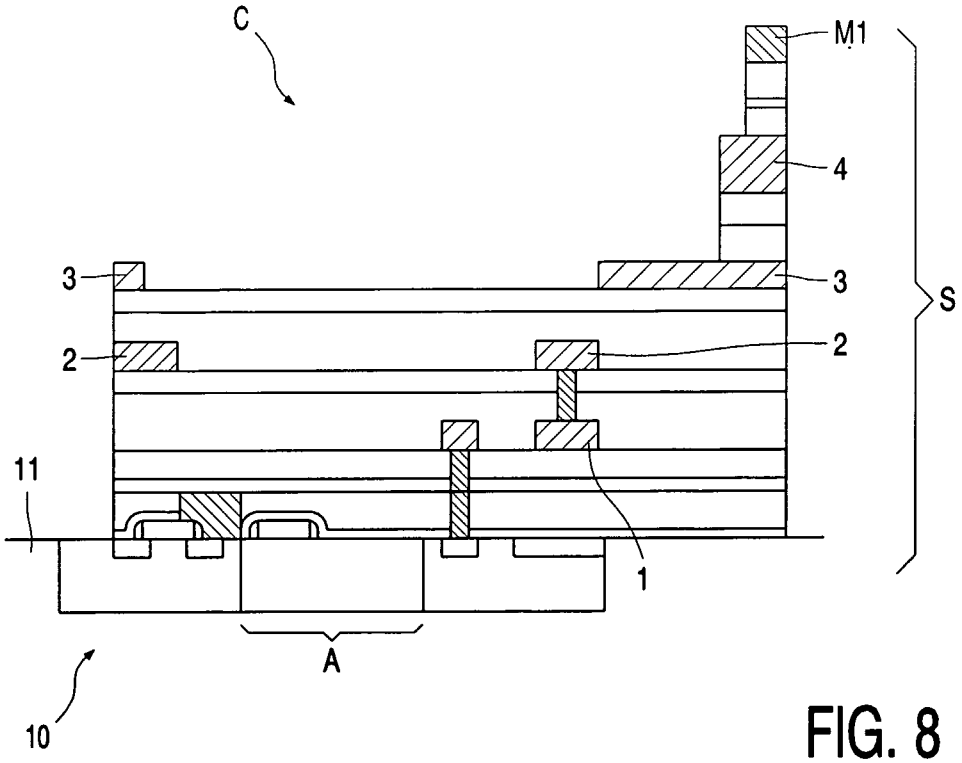

M1
9C
9B
9A
9
4
8B
8A
8
3
3
7B
7A
7
S
2
6B
6A
6
11
5D
5C
5B
5A
5
1
2
A
10

FIG. 7


C
M1
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3
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S
2
2
11
1
A
10

FIG. 8

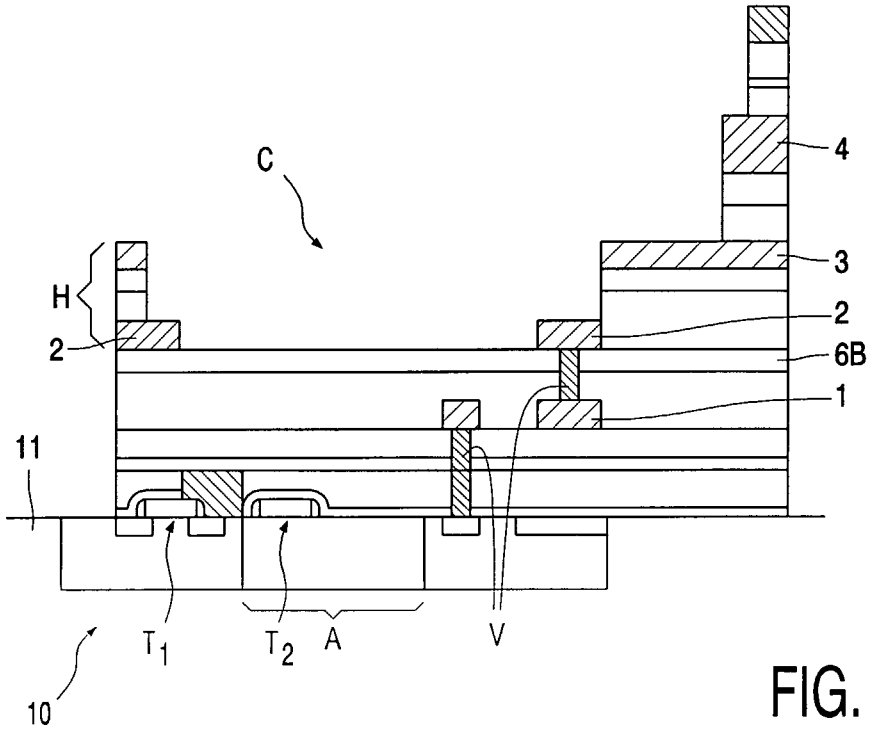


FIG. 9

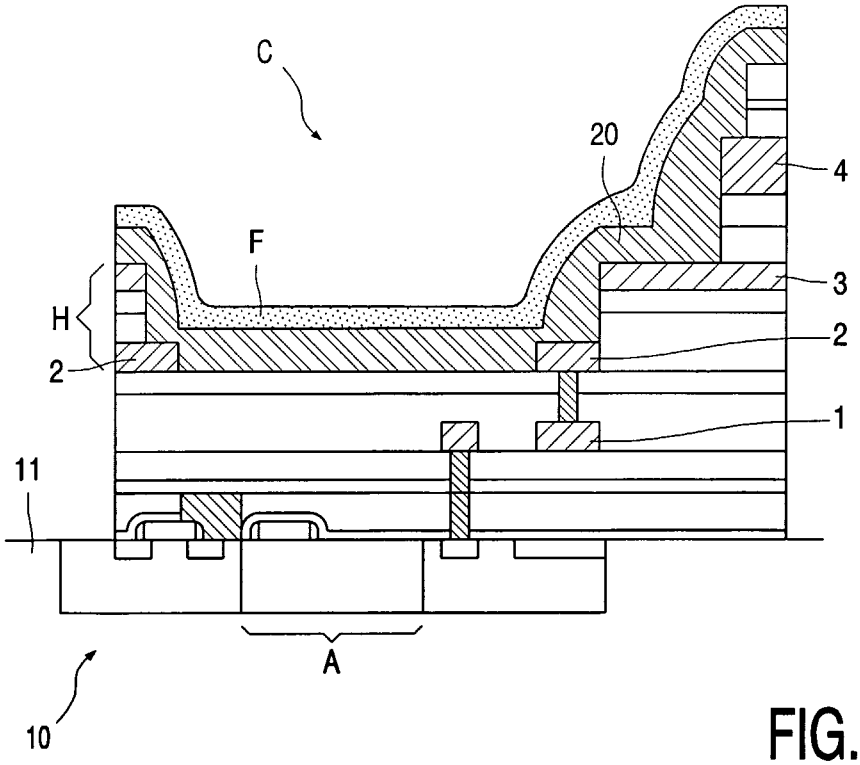
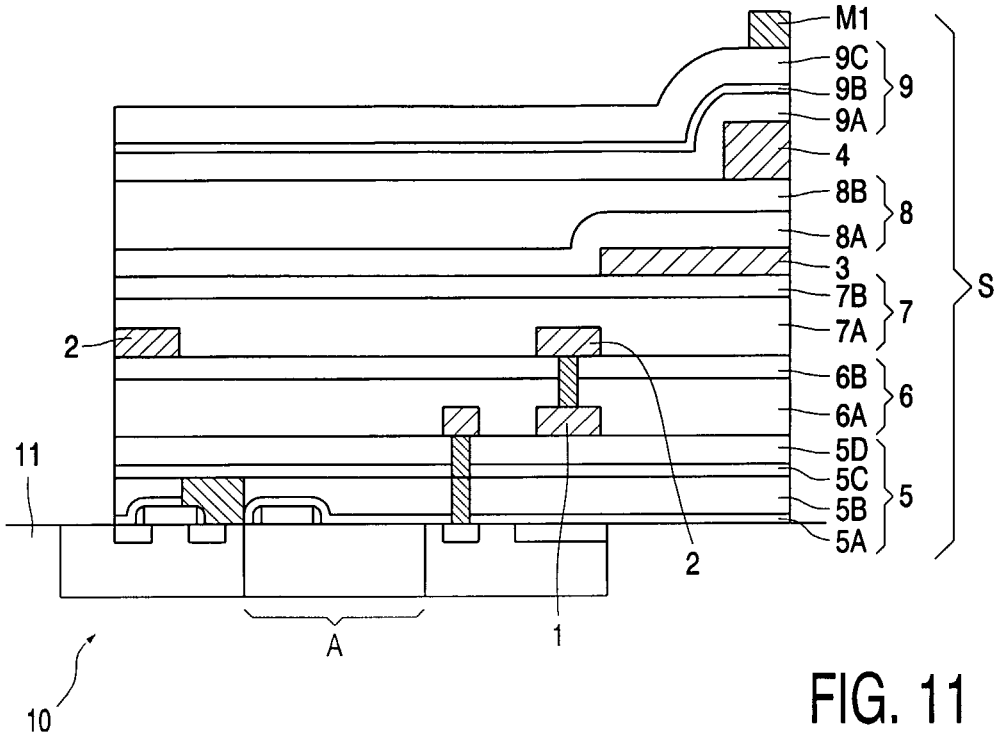


FIG. 10


M1
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9A
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8B
8A
8
3
7B
7A
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S
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6B
6A
6
11
5D
5C
5B
5A
5
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A
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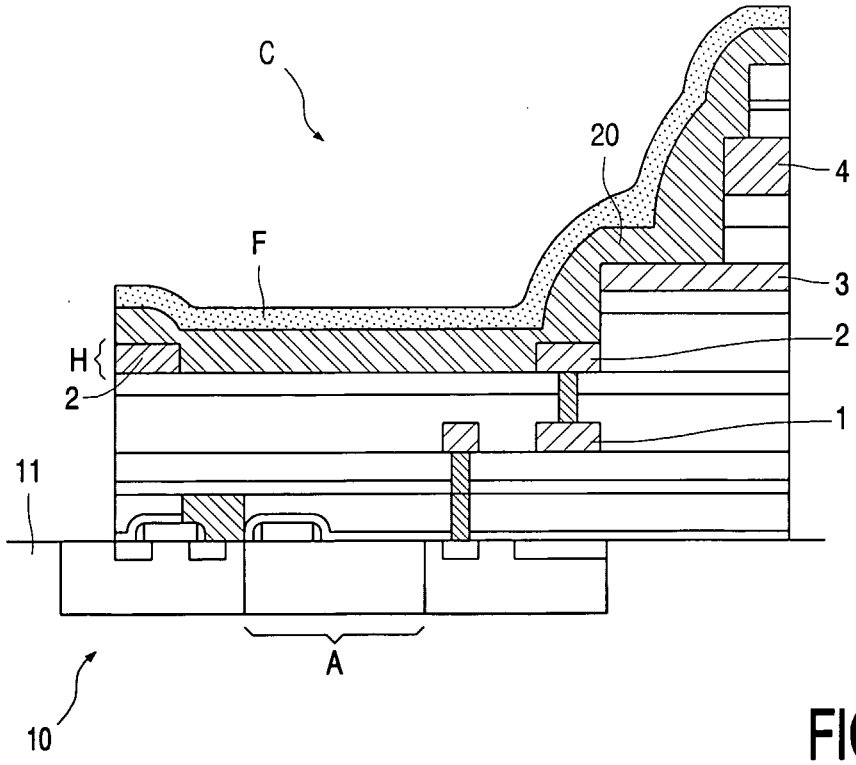
FIG. 11


C
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F
3
H
2
2
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11
A
10

FIG. 12

INTERNATIONAL SEARCH REPORT

Interi al Application No
PCT/IB2005/050360

A. CLASSIFICATION OF SUBJECT MATTER
IPC 7 H01L27/146 H01L31/0232

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
IPC 7 H01L

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)
EPO-Internal, PAJ, WPI Data

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category °	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
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X	PATENT ABSTRACTS OF JAPAN vol. 2002, no. 12, 12 December 2002 (2002-12-12) -& JP 2002 246579 A (SEIKO EPSON CORP), 30 August 2002 (2002-08-30) the whole document	1-13, 15-22

-/--

[X] Further documents are listed in the continuation of box C.

[X] Patent family members are listed in annex.

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Date of the actual completion of the international search	Date of mailing of the international search report
30 June 2005	13/07/2005

Name and mailing address of the ISA	Authorized officer
European Patent Office, P.B. 5818 Patentlaan 2 NL - 2280 HV Rijswijk Tel. (+31-70) 340-2040, Tx. 31 651 epo nl, Fax: (+31-70) 340-3016	Ley, M

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C.(Continuation) DOCUMENTS CONSIDERED TO BE RELEVANT

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