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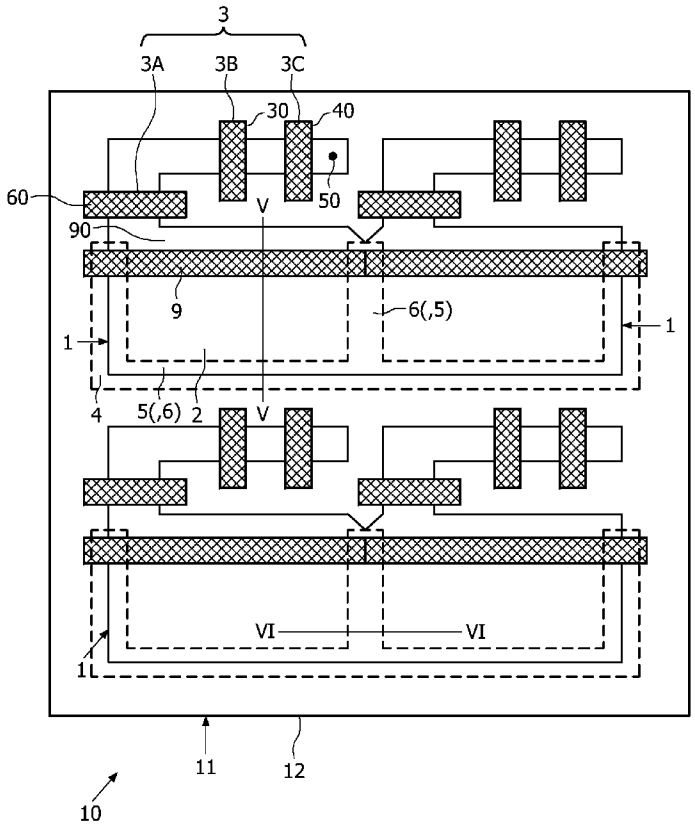
(54) Title: SEMICONDUCTOR DEVICE WITH AN IMAGE SENSOR AND METHOD FOR THE MANUFACTURE OF SUCH A DEVICE



(57) Abstract: The invention relates to a semiconductor device with a semiconductor body (12) with an image sensor comprising a two-dimensional matrix of pixels (1) each comprising a radiation-sensitive element (2) with a charge accumulating semiconductor region (2A) and coupled to a number of MOS field effect transistors (3), in which in the semiconductor body (12) an isolation region (4) is sunken for the separation of neighboring pixels (1) underneath which a further semiconductor region (5) with an enlarged doping concentration is formed. According to the invention the further semiconductor region (5) is sunken in the surface of the semiconductor body (12) and wider than the isolation region (4). Preferably the isolation region (4) is merely located there where a radiation sensitive element (2) borders on the MOS transistors (3) of a neighboring pixel (1) and there where two neighboring pixels (1) border on each other with their radiation sensitive elements (2) another sunken semiconductor region (6) with an enlarged doping concentration is located. Such a device (10) has a low leakage current and a large radiation sensitivity and charge storage capacity.

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Semiconductor device with an image sensor and method for the manufacture of such a device

The invention relates to a semiconductor device with a substrate and a semiconductor body with a semiconductor image sensor comprising a two-dimensional matrix of picture elements which include each a radiation-sensitive element coupled to a number of MOS field effect transistors for the benefit of reading the radiation-sensitive elements by selection means for selecting the picture elements, in which each radiation-sensitive element contains a semiconductor region of a first conductivity type in which charge carriers generated by incident radiation are accumulated and in which in the surface of a part of the semiconductor body laterally bordering on the semiconductor region, which part of the semiconductor body is of a second conductivity type opposite to the first conductivity type, an isolation region is sunk for separating neighboring picture elements and in which in the part of the semiconductor body of the second conductivity type underneath the isolation region a further semiconductor region of the second conductivity type is formed, having an increased doping concentration. Such a device is also called MOS image sensor and in practice usually called CMOS image sensor. Such a device can be manufactured in a relatively cost-effective manner and is attractive to many applications, more particularly for applications in the field of consumer electronics. The invention also relates to a method for the manufacture of such a device.

Such a device and method are known from patent specification US 2004/0094784 A1 published on May 20, 2004 under this number. It describes a CMOS image sensor having a pn-diode in a pnp-structure as a radiation-sensitive element. Moreover, each picture element has a number of MOS transistors for reading the picture elements while use is made of selection means. An n-type semiconductor region buried in the semiconductor body then operates as a charge accumulating region. In an adjacent (p-type) part of the semiconductor body there is an isolation region that is sunken relative to the surface of the semiconductor body and has the form of a what is called STI (Shallow Trench Isolation) region. Underneath is formed in the semiconductor body a buried p-type region having a higher doping concentration than that of the surrounding part of the (p-type) semiconductor

body. Because of this region the leakage current is reduced and the capacitance of the radiation-sensitive element is increased because it functions as a barrier for charge carriers i.e. electrons in the buried n-type semiconductor region.

A disadvantage of the known device is that the leakage current of the device is still relatively high and that the radiation sensitivity needs further improvement.

It is therefore an object of the present invention to provide a device and method which result in an improved leakage current and are extremely radiation-sensitive.

For this purpose a device of the type defined in the opening paragraph and in accordance with the invention is characterized in that the further semiconductor region is sunk in the surface of the semiconductor body and is wider than the isolation region. The invention is first and foremost based on the recognition that also the sides of the isolation regions contribute to an increase of the leakage current as a result of defects present there and that by sinking the further semiconductor region into the semiconductor body from the surface down and making it wider than the isolation region, the effect of the defects increasing the leakage current is reduced and hence the leakage current is reduced. The invention is further based on the recognition that a further designing and positioning of the further semiconductor region is possible without the need for additional process steps and there the desired object can be easily achieved by the use of an adapted mask, i.e. a mask having larger openings when the further semiconductor region is to be introduced, for example by means of ion implantation. Finally, the invention is based on the unanticipated recognition that with a device like this an increase of the radiation sensitivity is possible in a simple manner. Since the further semiconductor region, or rather a similar semiconductor region, can now provide the mutual separation of two neighboring picture elements also at a number of places, the use of an isolation region can be dispensed with at these places. This renders possible a smaller surface to be covered by the isolation function, so that the radiation-sensitive surface can be enlarged.

In a preferred embodiment of a semiconductor device according to the invention the isolation region is exclusively situated between two neighboring picture elements there where a radiation-sensitive element of one picture element borders on the MOS transistors of the other picture element, and there where two neighboring picture elements with their radiation-sensitive elements border on each other is found another semiconductor region of the second conductivity type having an increased doping

concentration and being sunk in the surface of the part of the semiconductor body. Since now - generally in one direction of the matrix - the isolation region is left out, the surface of the radiation-sensitive element can be enlarged. For a picture element having a dimension of 3.5 x 3.5 μm^2, said surface may be about 20% larger. An additional advantage is that the total length of the, for example STI isolation around a picture element can be smaller than that which results from an additional reduction of the leakage current.

With a periodical structure of the matrix of the image sensor the isolation region in one direction of the matrix may generally be left out or replaced with the other semiconductor region. In practice, where the radiation-sensitive element of the transistors belonging to a picture element is separated by a what is called transfer gate electrode, this will be the physical/geometrical longitudinal direction of this transfer gate eletrode, which direction is usually referred to as X-direction if the MOS image sensor is referred to as an XY MOS image sensor. In the other direction, i.e. the Y direction, in which the MOS transistors of the one picture element border on the radiation-sensitive element of a neighboring picture element, a sunken isolation region surrounded by the further semiconductor region is advantageously present.

In a number of cases it is possible that in both directions the sunken isolation regions are at least partly absent. If, for example, every third X-row of the matrix there is a reflection of the picture element orientation, where at the location of that reflection also in the Y direction two neighboring picture elements bound on each other with their radiation-sensitive elements, also at the location of that reflection, an isolation region may be left out in the Y direction and the separation of the picture elements may take place by the other semiconductor region formed there as well. Another case is the what is called shared concept case. The MOS transistors are then not present for each picture element, but they are used by a (small) number of neighboring picture elements, for example for a 2 x 2 picture element sub-matrix. In that case an isolation region may be left out and replaced with the other semiconductor region around, at any rate on three sides of, this sub-matrix and between the picture elements of the sub-matrix.

In an advantageous embodiment the further semiconductor region and the other semiconductor region are formed simultaneously. This renders its manufacture simple. Only a single masking step is needed.

Preferably, the further semiconductor region and the other semiconductor region are formed by means of a well-forming step from a CMOS process. Thus a standard process can be implemented. A modern CMOS process is of the what is called twin-tub type,

in which both an n-type and p-type well is formed in the semiconductor body. Depending on the fact whether the sensor has an n-type semiconductor region or a p-type semiconductor region for the accumulation of electrons and holes respectively, the p-well and the n-well step respectively can be used for this purpose. For further peripheral circuitry are preferably used both NMOS and PMOS transistors which are both available in a CMOS process.

Although also a LOCOS (Local Oxidation Of Silicon) may habe been used for the isolation region, the isolation region preferably comprises a what is called shallow groove isolation. Various advantages such as compactness and planarity are linked with this. Prefereably the first conductivity type is the n-conductivity type.

A method for the manufacture of a semiconductor device comprising a substrate and a semiconductor body with a semiconductor image sensor having a two-dimensional matrix of picture elements which comprise each a radiation-sensitive element coupled to a number of MOS field effect transistors for reading out the radiation-sensitive elements via selection means for selecting the picture elements, each radiation-sensitive element comprising a semiconductor region of a first conductivity type in which charge carriers generated by incident radiation are accumulated and in which an isolation region for separating neighboring picture elements is sunk in the surface of a part of the semiconductor body, which part laterally borders on the semiconductor region and is of a second conductivity type opposite to the first conductivity type and in which in the part of the semiconductor body of the second conductivity type underneath the isolation region a further semiconductor region of the second conductivity type is formed, having an increased doping concentration, which method is characterized according to the invention in that the further semiconductor region is sunk in the surface of the semiconductor body and is made wider than the isolation region. In this way a device according to the invention is obtained in a simple manner.

In a preferred embodiment of a method according to the invention the isolation region is formed only there where between two neighboring picture elements a radiation-sensitive element of one picture element borders on the MOS transistors of the other picture element and there where two neighboring picture elements are adjacent to each other with their radiation-sensitive elements another semiconductor region of the second conductivity type sunk in the surface of the part of the semiconductor body and having an increased doping concentration is formed. Preferably, the further semiconductor region and the other semiconductor region are formed simultaneously. The forming is preferably effected in a well-forming step from a CMOS process.

The invention will now be further explained with reference to several examples of embodiment and the drawing, in which:

Fig. 1 shows schematically and in plan view a known semiconductor device with an image sensor,

Figs. 2 and 3 show schematically and in cross section perpendicular to the thickness direction the device of Fig. 1 along the lines II-II and III-III respectively,

Fig. 4 shows schematically and in plan view a semiconductor device with an image sensor according to the invention, and

Figs. 5 and 6 show schematically and in cross section perpendicular to the thickness direction the device of Fig. 1 along the lines V-V and VI-VI respectively.

The Figures are not drawn to scale and some dimensions are shown in exaggerated form for clarity's sake. Corresponding regions or parts have as much as possible the same shading and the same reference character.

Fig. 1 shows schematically and in plan view a known semiconductor device with an image sensor. Figs. 2 and 3 show schematically and in cross section perpendicular to the thickness direction the device of Fig. 1 along the lines II-II and III-III respectively. The device 10 comprises for example (see Fig. 2) a substrate 11 and a semiconductor body 12 in which an image sensor is formed with a pixel matrix 1. The substrate and semiconductor body comprise a radiation-sensitive element 2 in which charge carriers generated by incident radiation are stored and transferred to a floating diffusion region 20 by means of a transfer electrode 9. The floating diffusion region 20 is coupled to a gate electrode 30 of a source-follower transistor 3B. The source-follower transistor 3B supplies an output signal to a row selection access transistor 3C with a gate electrode 40 for selectively gating the output signal to a connection 50. A reset transistor 3A with a gate electrode 60 serves to reset the floating diffusion region 20 to a certain charge level before charge is constantly transferred from the radiation-sensitive element 2.

The radiation-sensitive element 2 comprises (Fig. 2) an n-type semiconductor region 2A formed in a p-type region 12A of the semiconductor body 2, which n-type semiconductor region 2A runs as far as the transfer electrode 9 separated from the surface by a dielectric layer (not shown in the drawing). Thus the radiation-sensitive element 2

comprises a pnp structure and a what is called pinned photo diode. In the surface of the semiconductor body 12 (see Fig. 2 and Fig. 3) a sunken isolation region 4 is formed in the shape of a what is called shallow groove isolation surrounding the picture elements 1 (see Fig. 1). Underneath the isolation region 4 a buried further semiconductor region 5 is formed leading to a reduction of the leakage current of the device 10 and leading to an increase of the charge storage capacity of a radiation-sensitive element 2. This buried region 5 contains a higher (p-type) doping concentration than the surrounding p-type region 12A of the semiconductor body 12.

Fig. 4 shows schematically and in plan view a semiconductor device comprising an image sensor in accordance with the invention, and Figs. 5 and 6 show schematically and in cross section perpendicular to the thickness direction the device of Fig. 1 along the lines V-V and VI-VI. The main difference of the known device is formed by the positioning of the isolation region 4. At places where a picture element 1 (see Fig. 4) borders on an adjacent picture element 1 at the location of the radiation-sensitive elements 2 of these picture elements, the isolation region 4 is lacking (see also Fig. 6). At places where the transistors 3 of a picture element 1 border on the radiation-sensitive element 2 of an adjacent picture element (see also Fig. 5), the isolation region 4 is present, it is true, but there the further semiconductor region 5 is not a buried region like in the known device, but a region sunk in the surface of the semiconductor body 12 and, what is more, the width of the further semiconductor region 5 is larger than the width of the isolation region. This considerably improves the operation of the further semiconductor region 5, which results in a further reduction of the leakage current of the device 10 in accordance with the invention and a further increase of the charge storage capacity of the radiation-sensitive elements 2 of the device 10 in accordance with the invention.

In this example the doping concentration of the semiconductor region 2A is about 10^{17} at/cm^3. The doping concentration of the part 12A of the semiconductor body 12 is about 10^{15} at/cm^3. The doping concentration of the semiconductor region 2B is about 10^{10} at/cm^3 and the doping concentration of the further semiconductor region 5 is about 10^{17} at/cm^3.

In lieu of the isolation region 4 there is another semiconductor region 6 between two adjacent radiation-sensitive elements 2 of two neighboring picture elements (see Fig. 6), which other semiconductor region 6, just like the adjacent part 12A of the semiconductor body 12, is of the p-type, but has a higher doping concentration. By the lack of the isolation region at this spot (these kinds of spots) the radiation-sensitive element 2 of

the picture element 1 can be provided with a larger surface, for example for a pixel having a dimension of 3.5 μm this surface area can become 20% larger. This causes the sensitivity and the charge storage capacity of a pixel 1 to increase. The other semiconductor region 6 here provides an adequate separation between two neighboring picture elements 1. The doping concentration of the other semiconductor region 6 is about 10^{17} at/cm^3 in this example.

In his example the further semiconductor region 5 and the other semiconductor region 6 are formed simultaneously, in this case by means of ion implantation with a suitable mask. A well-forming step is selected from a what is called twin-tub CMOS process for the formation of these regions 5,6. In this step, which forms part of the CMOS process, further transistors are formed outside the region of the image sensor in the semiconductor body 12, which further transistors are not shown in the drawing and are both of the NMOST and the PMOST type. They form for example a circuit which provides driving and/or reading electronics. In an advantageous variant they (also) form part of a circuit for the purpose of image processing and/or image manipulation.

The pinned photodiode, which forms part of the radiation-sensitive element 2, is formed here between the buried n-type region 2A and a p-type region 2B sunken in the surface.

Manufacturing a device in accordance with the invention may be characterized with respect to the known method in the following manner. With the formation of the further semiconductor region 5, for example by means of implantation a mask is used, which is wider than the isolation region 4 and is aligned to it. The implantation energy(ies) and the associated doses are then selected such that the further semiconductor region 5 forms a region sunken in the surface. At the same time the mask is chosen such that the other semiconductor region 6 is formed simultaneously.

The invention is not restricted to the examples of embodiment given since within the scope of the invention many variations and modifications are possible for a man of skill in the art. For example, apart from CMOS also a Bi(C)MOS (Bipolar (Complementary) Metal Oxide Semiconductor) IC (Integrated Circuit) may be applied. In lieu of a radiation-sensitive element with an npn-structure, it is also possible for a radiation-sensitive element with a pnp-structure to be applied. Further it is observed that in lieu of the STI isolation regions also isolation regions obtained from the application of LOCOS (Local Oxidation Of Silicon) technology can be applied.

It is expressly stated that a radiation-sensitive element may not only be formed by a what is called pinned diode, but also differently, such as by a single non-pinned)

photodiode, in which the semiconductor region forms not more than a single pn-junction, for example with a semiconductor region of the opposite conductivity type positioned above it and bordering on the surface.

CLAIMS:

1. A semiconductor device (10) with a substrate (11) and a semiconductor body (12) with a semiconductor image sensor comprising a two-dimensional matrix of picture elements (11) which include each a radiation-sensitive element (2) coupled to a number of MOS field effect transistors (3) for the benefit of reading the radiation-sensitive elements (2) by selection means for selecting the picture elements, in which each radiation-sensitive element (2) contains a semiconductor region (2A) of a first conductivity type in which charge carriers generated by incident radiation are accumulated and in which in the surface of a part (12A) of the semiconductor body (12) laterally bordering on the semiconductor region (2A), which part (12A) of the semiconductor body (12) is of a second conductivity type opposite to the first conductivity type, an isolation region is sunk for separating neighboring picture elements and in which in the part (12A) of the semiconductor body (12) of the second conductivity type underneath the isolation region (4) a further semiconductor region (5) of the second conductivity type is formed having an increased doping concentration, characterized in that the further semiconductor region (5) is sunk in the surface of the semiconductor body (12) and is wider than the isolation region (4).

2. A semiconductor device (10) as claimed in claim 1, characterized in that the isolation region (4) is exclusively situated between two neighboring picture elements (1) there where a radiation-sensitive element (2) of one picture element (1) borders on the MOS transistors (3) of the other picture element (1), and there where two neighboring picture elements (1) with their radiation-sensitive elements (2) border on each other is found another semiconductor region (6) of the second conductivity type having an increased doping concentration and being sunken in the surface of the part of the semiconductor body.

3. A semiconductor device (10) as claimed in claim 2, characterized in that the further semiconductor region (5) and the other semiconductor region (6) are formed simultaneously.

4. A semiconductor device as claimed in claim 3, characterized in that the further semiconductor region (5) and the other semiconductor region (6) are formed by means of a well from a CMOS process.

5. A semiconductor device (10) as claimed in any one of the preceding claims, characterized in that the device comprises further field effect transistors, among which NMOS and PMOS transistors, located beyond the image sensor.

6. A semiconductor device (10) as claimed in any one of the preceding claims, characterized in that the isolation region (4) comprises a what is called shallow groove isolation.

7. A semiconductor device (10) as claimed in any one of the preceding claims, characterized in that first conductivity type is the n-type conductivity.

8. A method for the manufacture of a semiconductor device (10) comprising a substrate (11) and a semiconductor body (12) with a semiconductor image sensor having a two-dimensional matrix of picture elements (1) which comprise each a radiation-sensitive element (2) coupled to a number of MOS field effect transistors (3) for reading out the radiation-sensitive elements (2) via selection means for selecting the picture elements (1), each radiation-sensitive element (2) comprising a semiconductor region (2A) of a first conductivity type in which charge carriers generated by incident radiation are accumulated and in which an isolation region (4) for separating neighboring picture elements (1) is sunk in the surface of a part (12A) of the semiconductor body (12), which part laterally borders on the semiconductor region (2A) and is of a second conductivity type opposite to the first conductivity type and in which in the part (12A) of the semiconductor body (12) of the second conductivity type underneath the isolation region (4) a further semiconductor region (5) of the second conductivity type is formed, having an increased doping concentration, characterized in that the further semiconductor region (5) is sunk in the surface of the semiconductor body (12) and is made wider than the isolation region (4).

9. A method as claimed in claim 8, characterized in that the isolation region (4) is formed only there where between two neighboring picture elements (1) a radiation-sensitive element (2) of one picture element (1) borders on the MOS transistors (3) of the other picture

element (1) and there where two neighboring picture elements (1) are adjacent to each other with their radiation-sensitive elements (2) another semiconductor region (6) of the second conductivity type is formed, sunken in the surface of the part (12A) of the semiconductor body (12) and having an increased doping concentration.

10. A method as claimed in claim 9, characterized in that the further semiconductor region (5) and the other semiconductor region (6) are formed simultaneously.

11. A method as claimed in claim 9 or 10, characterized in that the further semiconductor region (5) and the other semiconductor region (6) are formed by means of a well-forming step from a CMOS process.

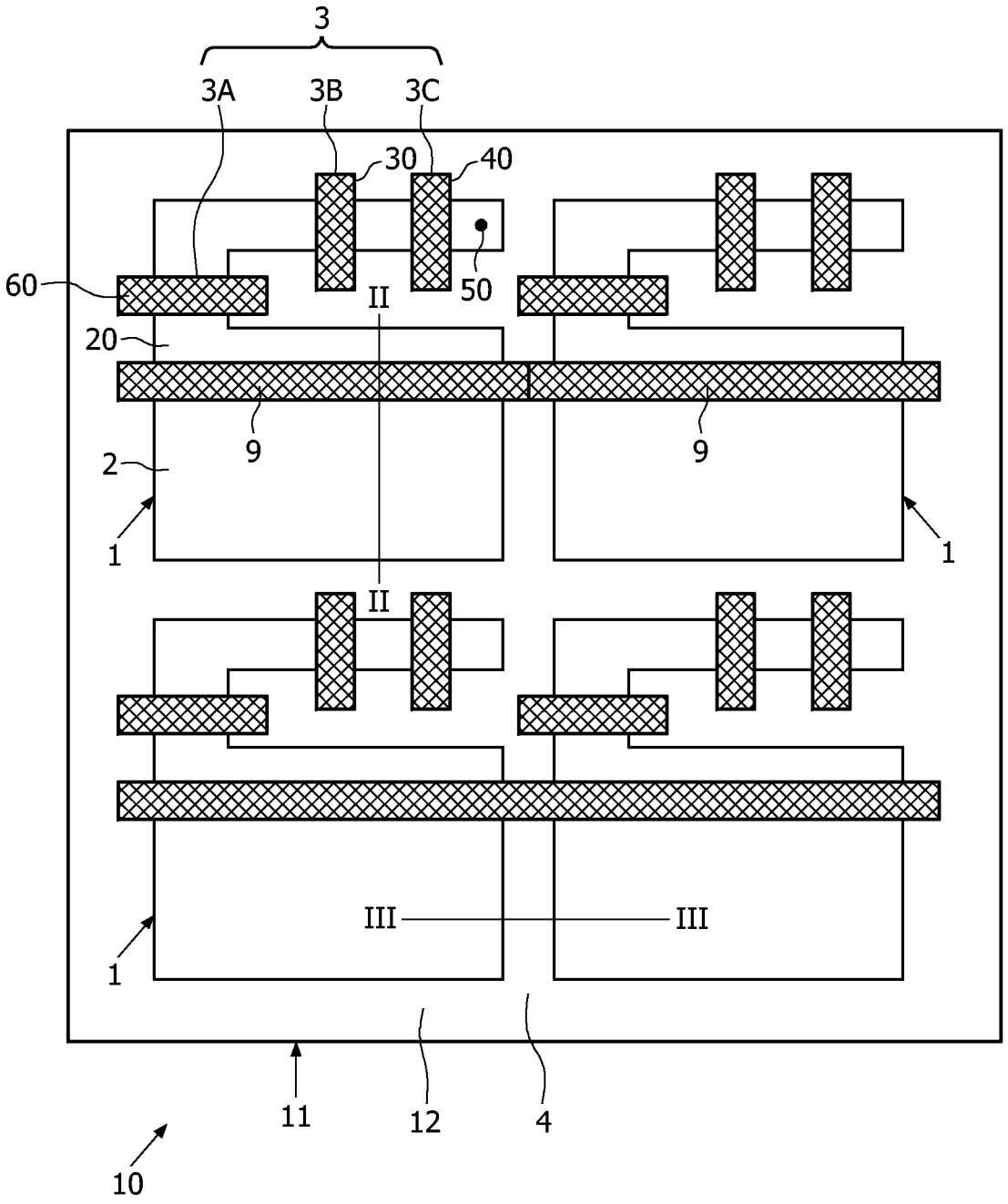

FIG. 1

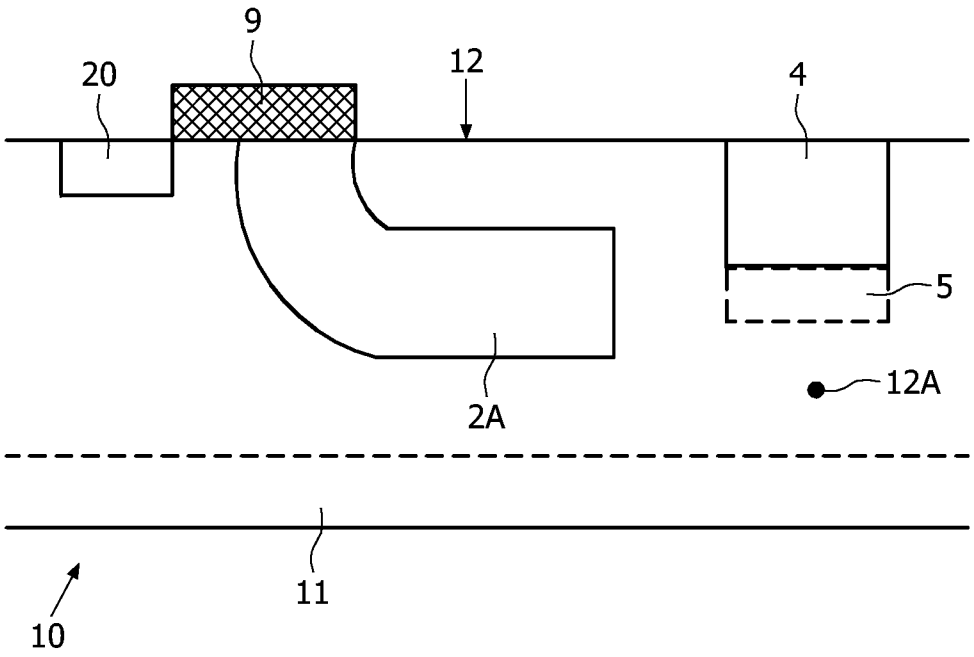

FIG. 2

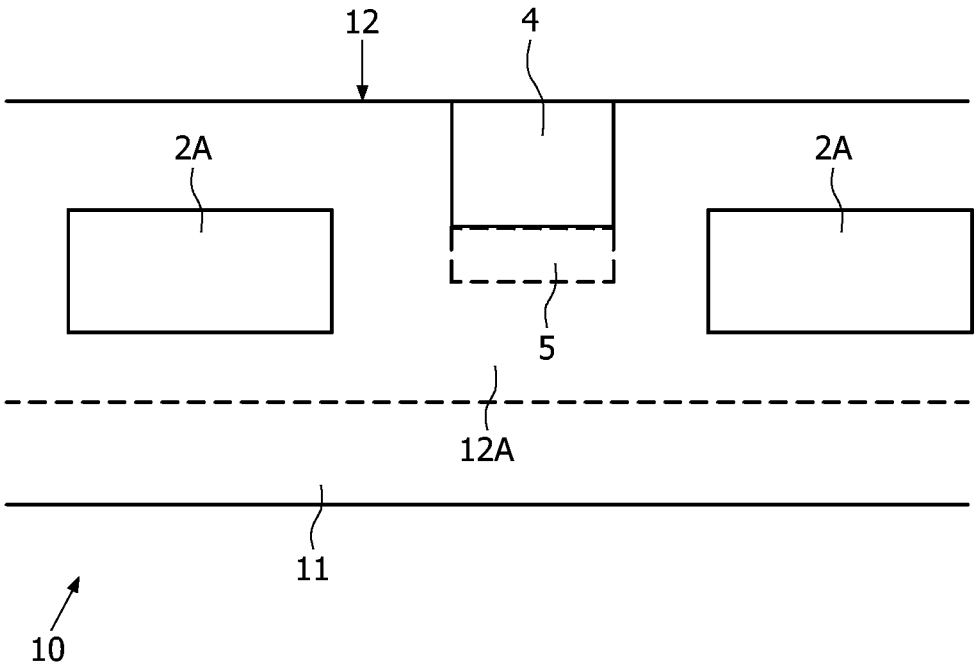

FIG. 3

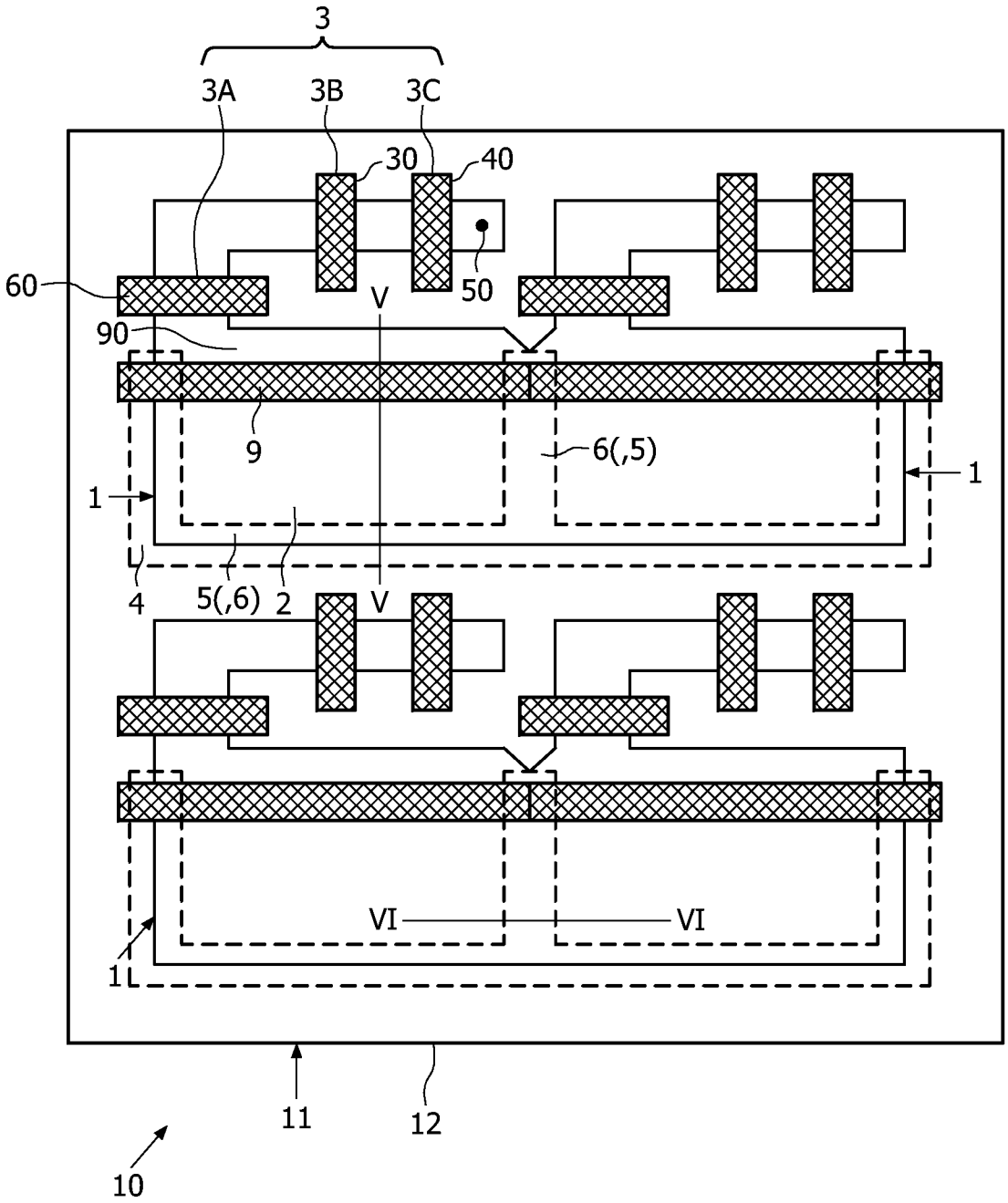

FIG. 4

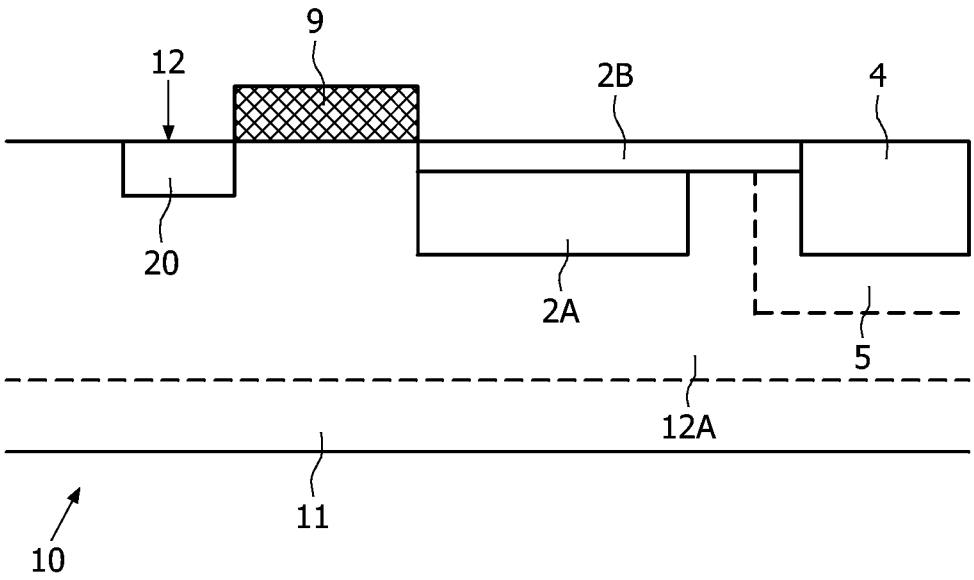

FIG. 5

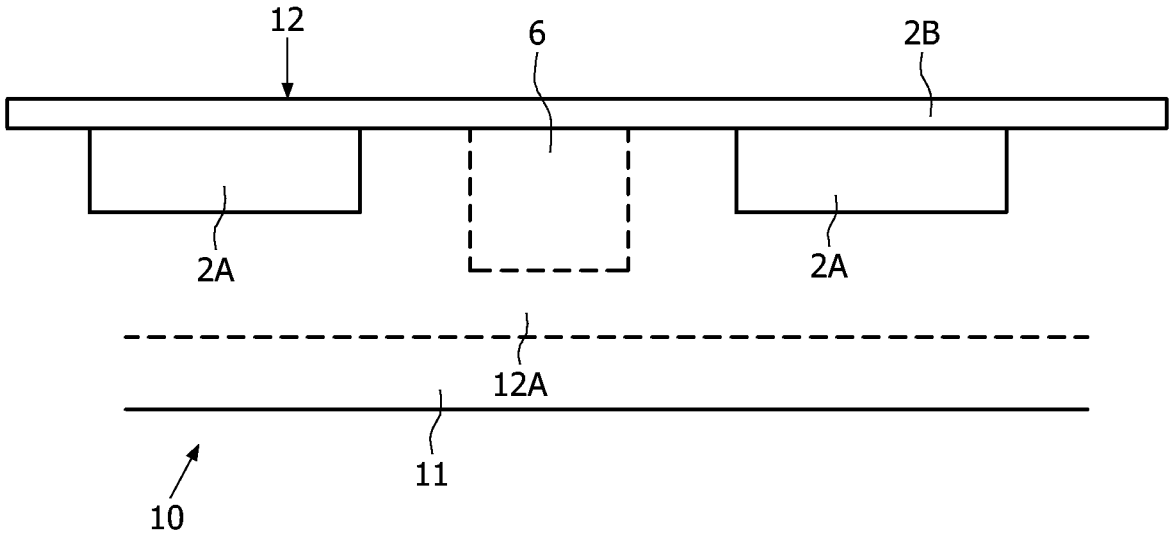

FIG. 6

INTERNATIONAL SEARCH REPORT

International application No
PCT/IB2006/051301

A. CLASSIFICATION OF SUBJECT MATTER
INV. H01L27/146

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
H01L

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)
EPO-Internal, PAJ, INSPEC

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	PATENT ABSTRACTS OF JAPAN vol. 2003, no. 12, 5 December 2003 (2003-12-05) -& JP 2003 234496 A (SONY CORP), 22 August 2003 (2003-08-22) abstract; figures 3-5,8,9	1-9,11
X	US 2003/038336 A1 (MANN RICHARD A) 27 February 2003 (2003-02-27) paragraphs [0020] - [0026]; figures 1-5	1,5-8
A	US 5 970 316 A (MERRILL ET AL) 19 October 1999 (1999-10-19) figures 8-10	1-11

☐ Further documents are listed in the continuation of Box C.

☒ See patent family annex.

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INTERNATIONAL SEARCH REPORT

Information on patent family members

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Patent document cited in search report	Publication date	Patent family member(s)	Publication date
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US 2003038336 A1	27-02-2003	WO 03019675 A1 US 2004021194 A1	06-03-2003 05-02-2004
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